DESIGN OF SQUARE ROOT CARRY SELECT ADDER USING CARRY SAVE OPERATION

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ABSTRACT

Carry select adder and Carry save adder is designed to speed up arithmetic operations and to reduce the computation time. Both adders are the high speed adders. Carry select adder is used to perform fast arithmetic functions faster in data processing processors. Reduced area, reduced delay, increased speed and low power consumption are the most important features of the modern electronic system design. In this proposed work 4-bit Square Root Carry Select Adder (SQRT CSLA) constructed using Carry save operation. Here Ripple Carry Adder (RCA) operation is replaced by Carry Save Adder (CSA) operation and 4:1 Multiplexers are used in this design. So it is reliable in terms of power and delay. In this 4-b SQRT CSLA constructed using Carry save operation design power consumption and delay are reduced compared with the Regular SQRT CSLA and Modified SQRT CSLA. In this work performance is evaluated through the logic design and layout in 0.12µm CMOS process technology.

KEYWORDS: Low power consumption, less delay, Carry save operation, DSCH (Digital schematic).

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INTRODUCTION

For VLSI design basic requirements are low power consumption, compactness of the design and speed. Low power will improve reliability, reduced area will improve portability, if the delay is reduced speed will be improved. Addition is the basic operation of VLSI design. In adder speed is limited by time sum of all the bit position is generated after previous bits are computed and carry is propagated into next position. CSLA and CSA are high speed adders which are designed mainly to solve the problem of carry propagation delay. Here carryout of each section determines the carrying of next section. Then select a carry to generate sum and carry at next section [1]. CSLA and CSA are used in the digital signal processor and several data processing applications.

This paper presents a comparison of 4-bit SQRT CSLA constructed using Carry save operation, 4-bit Regular CSLA, 4-bit Modified SQRT CSLA. In this work proposed 4-bit SQRT CSLA constructed using Carry save operation shows less power and less delay compared with other two CSLA. This paper organized as following sections: Section I deals with Introduction. Section II deals with literature survey. Section III explains about Regular SQRT CSLA. Section IV explains about the modified SQRT CSLA. Section V deals with the proposed SQRT CSLA constructed using Carry save operation. Results are analysed in section VI and section VII concludes.

LITERATURE SURVEY

Many researchers have been done regarding the optimization of low power area efficient carry select adder with standard CMOS logic.

Existing carry select adder which is 64-bit CSLA intends high performance & low power applications [9]. The modified CSLA which contains add one circuit and inverter elimination in carry path, which minimize delay than regular CSLA [13]. CSLA which is used to minimize delay here contains two additions done in half of the cycle and sharing is accomplished by latches [14]. In the CSLA replace any one Ripple Carry Adder (RCA) structure when enable=1 then RCA structure calculate for Cin=1 that result is stored in D-latch. When enable=0 then D-latch and full adder output is given to multiplexer as input [6].

Carry Save Adder (CSA) computes multiple numbers. Here in the Carry save operation Sum and carry computed separately. Delay is reduced here [16]. Optimizing transformations using operation- duplication and operation split concepts in this CSA. Because of its faster timing and less area these CSA is used in register transfer design in industries [17].

4-BIT REGULAR SQRT CSLA
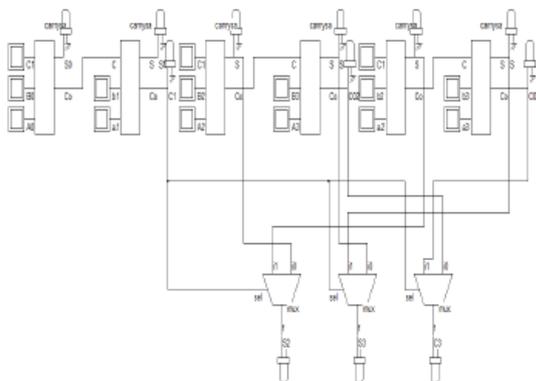
Regular SQRT CSLA with structure contains 2 blocks

Fig. 1 shows circuit of 4-bit Regular SQRT CSLA.

Fig.1. Circuit for 4-bit Regular SQRT CSLA to the MUX in the block 2. To select the other output bits and two sum out bits S0 and S1.This output carry C0 is given as the produce S0 and F.A produce S1 carry is fed as select

line to MUX in block 2, select input to the MUX in the block 2. To select the other output bits. Block 2 contains two RCA blocks. Both blocks are provided with same inputs bits and carry input for one RCA block is Cin = 0 and other RCA Cin=1. The outputs

Block 2 contains one RCA block which is similar to the Block 1, 3-bit BEC and 3 MUX. Here outputs obtained are S2, S3and C3. Modified 4-bit SQRT CSLA circuit is shown in the Fig. 2 determined are S2, S3 .Hence carry out bit is C3. It also contains three 2:1 multiplexers for selecting outputs sum and Binary to Excess one Converter (BEC) which is used in SQRT CSLA instead of using RCA with Cin =1. It reduces the delay [1]. BEC consists of 3 basic logic carry

4-BIT MODIFIED SQRT CSLA

Block 1 is a RCA block which contains one FA and one Half adder. H.A functions NOT, AND and XOR. 4-bit

BEC operations are expressed as

$$a0 = b0$$

$$a1 = b0{\wedge}b1$$
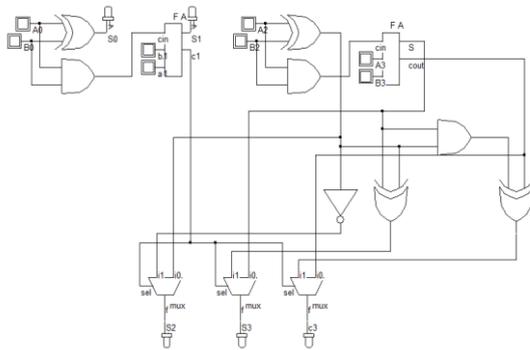
$$a2 = b2{\wedge}(b0\&b1)$$

$$a3 = b3{\wedge}(b0\&b1\&b2)$$

Fig.2. Circuit for 4-bit Modified SQRT CSLA

In this SQRT CSLA MUX get input from output of RCA which Cin=0 and BEC. Then it selects the sum & carry based on the carry from the previous stage. 4-bit binary to excess one converter circuit is shown in the Fig. 3.
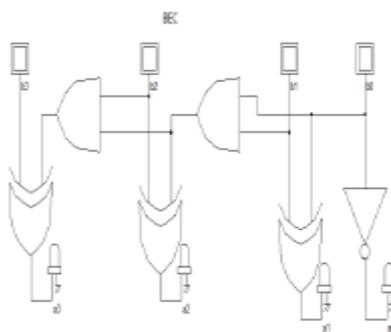

Fig.3. Circuit 4-bit Binary to excess one converter

PROPOSED WORK

4-BIT SQRT CSLA CONSTRUCTED USING CARRY SAVE OPERATION

This proposed 4-bit SQRT CLSA constructed using carry save operation structure contains 6 block.

Block 1 and Block 2 are Carry Save Adder (CSA) blocks. RCA in the modified SQRT CSLA is replaced by this CSA Carry save operation performs high speed addition operation by computing sum and carry separately at each stage. Then at the last stage final sum and carry are computed [16].

Here in block 1 and block 2 four terms are taken as the inputs x_0, x_1, y_0, y_1, z_0, z_1, w_0,w_1. Outputs are determined as sum s_0,s_1 and carry output as c_0,c_1. This carry outputs are fed as the select inputs for the multiplexers in the block 6. 2-bit CSA adder circuit is shown in the Fig. 4

Block 2 inputs are x_2, x_3, y_3, y_4, z_3, z_4, w_2, w_3. Outputs are determined as sum s_{02}, s_{03} and carry c_{02}, c_{03}. These four output bits were fed as the input to the block 3 4-bit BEC. Block 3 outputs are fed as the input to block 4 4-bit BEC. Block 5 outputs are fed as the input to block 5 4-bit BEC.

Block 6 contains four 4:1 multiplexers, which has two select inputs and 4 inputs.

(a)If select input is 00 output of block 2 is obtained as finial output, (b)If select input is 01 output of block 3 is obtained as finial output.

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(c)If select input is 10 output of block 4 is obtained as finial output.

(d)If select input is 11 output of block 5 is obtained as finial output. Multiplexers gets inputs form the output of blocks 2, 3, 4 and 5.

Four finial outputs were selected based on the following conditions listed below

Hence finial output is obtained as sum s2, s3 and carries c2, c3.Circuit for proposed 4-bit SQRT CSLA constructed using carry save operation is shown in the Fig.5.
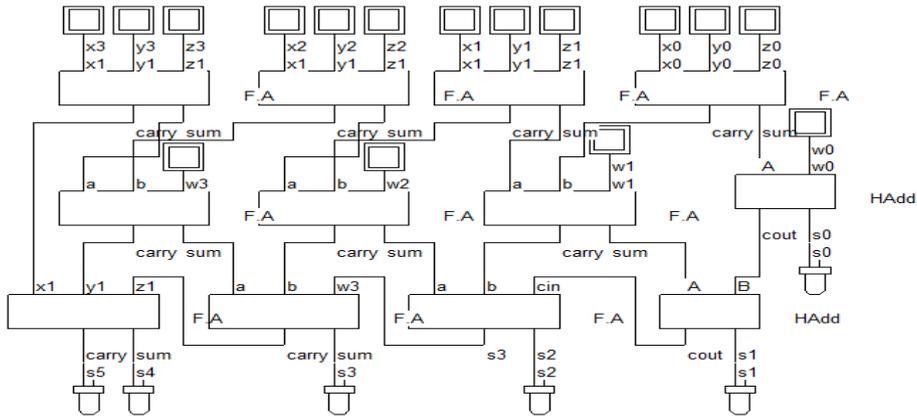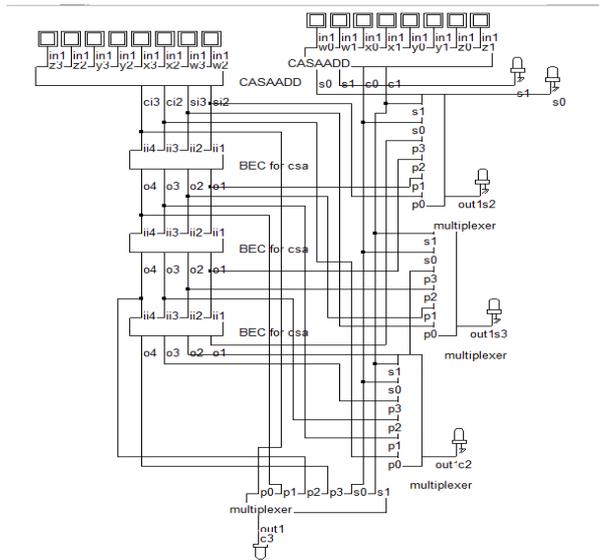

Fig.4. Circuit for carry Save Adder

Fig.5. Circuit for proposed 4-bit SQRT CSLA

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RESULTS AND COMPARISONS

Power consumption and delay are determined for proposed 4-bit SQRT CSLA constructed using carry save operation. Power Consumption and delay are reduced compared for proposed method compared with the regular and modified SQRT CSLA. This is simulated by using the microwind 2 version.

Technology used is CMOS 0.12μm Technology. Results obtained by simulation are mentioned in the Table 1. The simulation waveform obtained for the proposed 4-bit SQRT CSLA constructed using carry save operation is shown in the Figure 6.

TABLE 1: COMPARISON OF SQRT CSLA'S

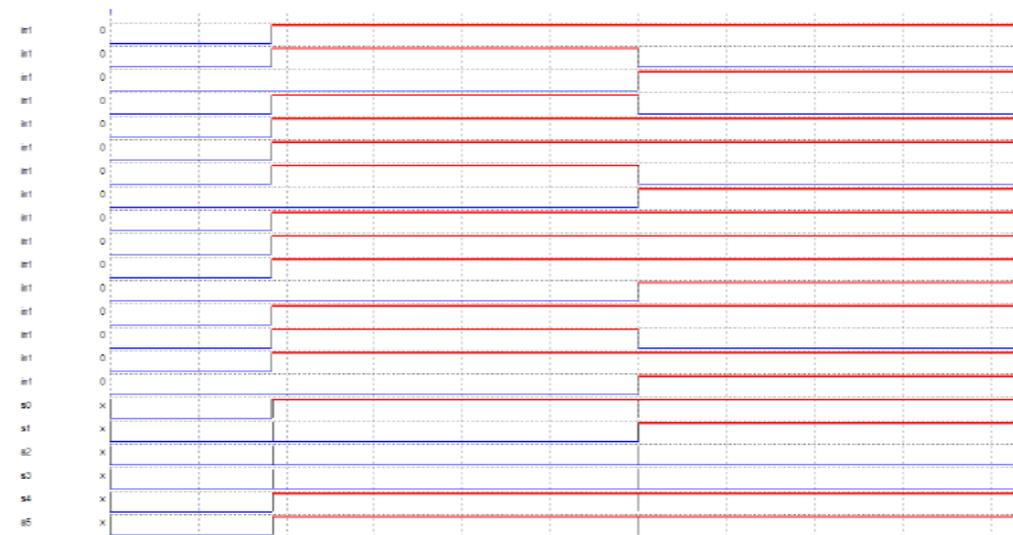| Word size 4-bit	Power consumption (μW)	Delay(ns)
Regular SQRTCSLA	72.128	19.890
Modified SQRT CSLA	61.788	16.981
Proposed SQRT CSLA constructed using carry save operation	14.631	1.510

Fig.6. Timing wave for Proposed 4-bit SQRT CSLA constructed using carry save operation.

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CONCLUSION

In this proposed work the SQRT CSLA constructed using Carry save operation using a simulated microwind tool. Power consumption of 4-bit SQRT CSLA constructed using Carry save operation is 57.5% and 47.17% lesser than regular and modified SQRT CSLA. Delay is also reduced in this proposed SQRT CSLA. This proposed work can be done for the 16-bit, 32-bit and for 64-bit SQRT CSLA based on their applications. For the future work area may be reduced. Hence the proposed square root carry select adders consume less power compared to other carry select adders. Thus the proposed SQRT CSLA performance is improved in terms of power and delay.

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