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DESIGN OF TESTABLE REVERSIBLE SEQUENTIAL CIRCUITS FOR DETECTING FAULTS USING TOFFOLI AND PERES GATES

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ABSTRACT

Reversible logic function has become an important research area and its applications are used in quantum computing, low power CMOS, nanotechnology, quantum dot cellular automata and optical computing. Reversible circuits are implemented using reversible gates. Reversible logic is mostly used due to its less heat dissipation. The design of reversible sequential circuits using Toffoli and Peres gates are proposed. The circuit can be tested for classical unidirectional stuck-at faults using only two test vectors and provides better fault coverage. The proposed Toffoli and Peres gate surpasses the Fredkin gate and Multiplexer Conservative QCA gate in terms of area, delay, majority voters. The simulation is done using Modelsim and performance is computed using Xilinx tool.

KEYWORDS: Reversible computing, Fredkin gate, MX-CQCA, Toffoli gate, Peres gate

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INTRODUCTION

Energy dissipation is one of the major issues in present day technology. Energy dissipation due to information loss in high technology circuits and systems constructed using irreversible hardware was demonstrated by R.Landauer. According to Landauer's principle, the loss of one bit of information dissipates kTln2 joules of energy where k is the Boltzmann's constant and T is the absolute temperature. Later Bennett showed that in order to avoid kTln2 joules of energy dissipation in a circuit it must be built from reversible circuits.

A reversible logic circuit should use minimum number of reversible gates, garbage outputs, and constant inputs. The key insight of reversible computing is that information does not need to be destroyed during computation. These reversible circuits can generate a unique output vector from each input vector and vice versa that is, there is one-to-one mapping between input and output vectors. Thus an N*N reversible gate can be constructed as

IV= (I1,I2,13,..........,IN)

OV=(O1,O2,O3,........,ON)

Where IV and OV represents the input and output vectors respectively.

A reversible logic gate is a k-input, k-output device that maps each possible input pattern into a unique output pattern. While constructing reversible circuits with the help of reversible gates, some restrictions should be strictly followed: Fan out is not permitted and Loops is not permitted.

Synthesis of reversible logic is significantly different from conventional logic synthesis. Since loops are not permitted, a reversible logic circuit can be specified as a simple sequence of gates. Further since fan out is not permitted and assuming an appropriate technology, a reversible logic circuit can realize the inverse specification simply by applying the gates in the reverse order. Hence, synthesis can be carried out from the inputs towards the outputs or from the outputs towards the inputs.

Zero energy dissipation would be possible only if the network consists of reversible gates. The advantages of Quantum dot cellular automata over conventional circuitry are extremely small size, high density, low power requirements and high processing speeds.

The paper presents the design of sequential circuits using Fredkin, MX-CQCA,

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Toffoli and Peres gate respectively. This paper is organised as follows: Section II deals with background behind the research work. Section III presents the existing Fredkin and MX-CQCA gate. Section IV presents the proposed Toffoli and Peres gate. Section V describes the design of Reversible latches using Toffoli and Peres gate. Section VI presents the design of Negative enable Reversible D latch using Toffoli and Peres gate. Section VII presents the design of master slave D flip flops using Toffoli and Peres gate. Section VIII presents the design of DET flip flops using Toffoli and Peres gate. Section IX presents the design of Fredkin equivalent circuit. Section X presents the design of MX-CQCA equivalent circuit. Section XI presents the design of proposed toffoli equivalent circuit. Section XII presents the design of proposed Peres gate equivalent circuit. Section XIII deals with results and discussion. Section XIV provides the conclusion.

BACKGROUND

Few objectives need to satisfy the reversible circuit. There are number of gates; minimize the number of garbage outputs and Synthesis. Various researches had been studied in reversible logic. Feynman gate, New gate and Fredkin gate are used for reversible logic synthesis [3]. Piston and Frank introduced their reversible logic operations [4]. In reversible gates, any Boolean function can be utilized [5]. Reversible logic is used for many applications like quantum computing. Algorithm is presented to synthesize reversible functions. In reversible functions, the algorithm was positive polarity reed Muller expansion to synthesize the function of Toffoli gates [6]. Few problems faced by reversible logic synthesis are fanouts not allowed and feedback from gate output to inputs is not allowed. CMOS implementations of reversible gates are proposed [7]. The designs of reversible sequential circuits are introduced to minimize the quantum cost and delay number of garbage outputs[12]. Various New reversible logic gates are introduced using Boolean expansion [12].

EXISTING FREDKIN AND MX- CQCA GATE

A conservative logic gate is a multiple-output logic element in which the number of ones at the inputs is equal to that of the corresponding outputs. Fredkin gate is a 3*3 input output reversible gate.

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Any stuck-at-1 fault in the conservative logic circuit can be detected by setting all inputs to 0s followed by subsequent checking of the outputs for the presence of any 1s. Any stuck-at-0 fault can be detected by setting all inputs to 1s followed by subsequent checking of the outputs for the presence of any 0s.

The Fredkin gate is a popularly used reversible conservative logic gate. The Fredkin gate can be described as a mapping (A,B,C) to (P = A, Q =A'B + AC, R = AB + A'C) where A, B, C are the inputs and P,Q,R are the outputs respectively. The truth table for the Fredkin gate demonstrates that Fredkin gate is reversible and conservative in nature, it has unique input and output mapping and also has the same number of 1s in the outputs as in the inputs.

Table 1.Truth table of Fredkin gate

A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	1	0
1	1	0	1	0	1
1	1	1	1	1	1

Table 2. Truth table of MX-CQCA gate

A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	0	1
0	1	1	0	1	1
1	0	0	0	1	0
1	0	1	0	1	1
1	1	0	1	0	1
1	1	1	1	1	1

The output equations of the reversible gates are used as templates for mapping the characteristic equation of the latch into an equivalent reversible design. This design methodology includes the design of D latches and D flip flops.

MX- cqca has one of its outputs working as a multiplexer, which will help in mapping the sequential circuits based on it, while the other two outputs will work as AND and OR gates respectively. The mapping of the inputs to outputs of the MX- cqca is: P = AB, Q = AB' + BC, R = B +C, where A, B and C are the inputs and P,Q,R are the outputs respectively. Fredkin and MX-CQCA gates are designed using HDLQ Verilog library for performing the fault testing.

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PROPOSED TOFFOLI AND PERES GATE

Toffoli gate invented by Tommaso Toffoli is one of the universal reversible logic gate. A, B, and C are the inputs to Toffoli gate and P, Q, R are the outputs. When two bits are set, it alters the third bit otherwise all remain the same. Peres gate has three inputs and outputs. Each input is mapped to the each output (P=A, Q = A XOR B R = AB XOR C). It has the quantum cost of 4.

Table 3. Truth table of Toffoli gate

A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	0	1
1	1	0	1	1	1
1	1	1	1	1	0

Table 4. Truth table of Peres gate

A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	1	0
1	0	1	1	1	1
1	1	0	1	0	1
1	1	1	1	0	0

DESIGN OF REVERSIBLE LATCHES USING TOFFOLI AND PERES GATE

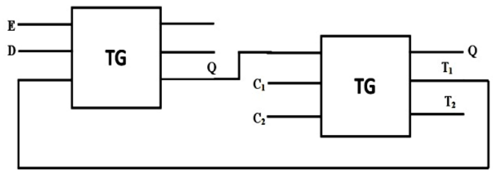

Fig 1. Reversible D latch with Control signals using Toffoli gate

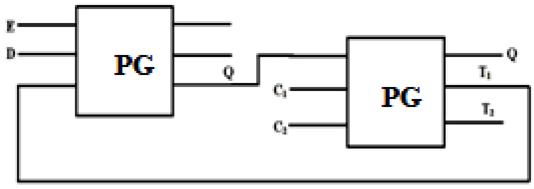

Fig 2. Reversible D latch with control signalsusing Peres gate

Enable E and D are the input signals to the D latch in Toffoli gate and P, Q, R are the output signals. When the enable is zero the value of D is passed to the output Q and R. When the enable is one, the value of D is passed to the output P and Q (latch maintains the previous state of Q). Latch is tested with control signals C1, and C2, when C1C2 = 01, the latch works as fault free mode in Toffoli and Peres gate. When C1C2 = 00 or 11, the latch works as test mode in Toffoli and Peres gate. In both these modes, there is a shift in the

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output waveform and latch is tested for various modes of operations.

DESIGN OF NEGATIVE ENABLE REVERSIBLE D LATCH USING TOFFOLI AND PERES GATE

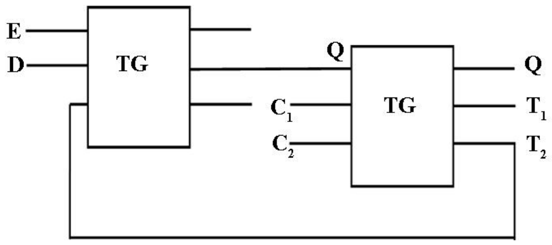

Fig 3. Negative enable D latch using Toffoli gate

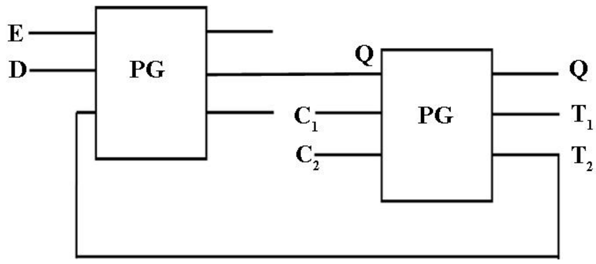

Fig 4. Negative enable D latch using Peres gate

The latch is tested with various values of enable, D signals latch works in normal mode or test mode depends upon the value of control signal.

DESIGN OF MASTER SLAVE D FLIP FLOPS USING TOFFOLI AND PERES GATE

In previous work, master slave flip flops are designed using Fredkin gate. The proposed work is based on Toffoli and Peres gate.

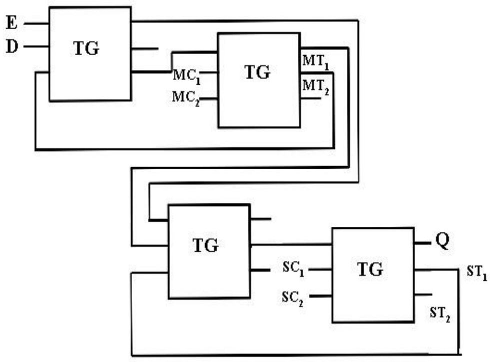

Fig 5. Master slave D flip flop using Toffoli gate

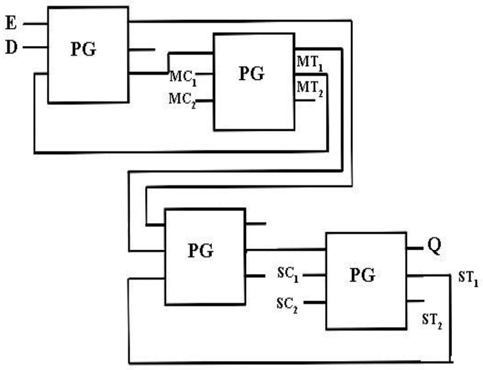

Fig 6.Master slave D flip flop using Peres gate

Four Peres gate and Toffoli gate are used in master slave D Flip-flops. When enable is zero, the value of D is passed to output Q otherwise it maintains the previous state. mC1, mC2, SC1, SC2 are the control modes for the master latch and slave latch. In normal mode,

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when enable and D value are one, output of D is passed to Q. In test mode, when all control signals are zero, when enable is one, the value of D is reflected to the output Q. Master slave flip flop is tested for two modes of operations.

Four Toffoli gates or Four Peres gates are used two Toffoli or Peres gate acts as master latch, while lower two Toffoli or Peres gate acts as a slave latch. mC1,mC2,sC1,sC2 form the control signals for master latch and slave latch. Latch is tested under the fault free mode and test mode. Toffoli or Peres gate at the end acts as the 2:1 MUX.

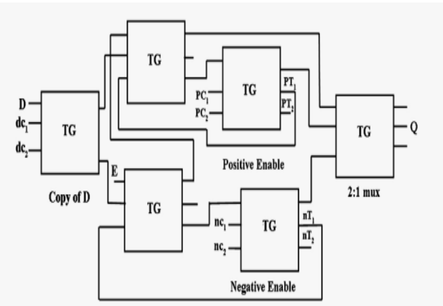

Fig 7. DET flip flops using Toffoli gate

DET based Toffoli gate or Peres gate works in two modes of operation. In normal mode, the value of nc1 and nc2 is 0 and 1. In test mode, the value of pc1 and pc2 is either 0 or 1. By setting all control signals as zero, when enable is one, the output Q is zero. When enable and D value are one, all control signals as zero, the output Q is one. Latches are tested for various inputs of control signals and enable values.

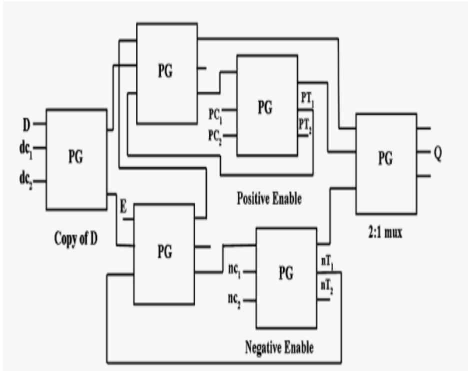

Fig 8. DET flip flops using Peres gate

FREDKIN GATE EQUIVALENT CIRCUIT

The QCA design of the Fredkin gate is shown in fig 9 represents the QCA cell and the QCA logic devices. It consists of fan-outs, inverters, cross wires, L-shaped wires and majority voters. QCA layout of the Fredkin gate requires six FOs, two INV, five CWs, seven LSs and six MJs. This design is based on the Landauer four phasing clocking scheme. The clocking zones are shown by D0, D1, D2 and D3.

The QCA design of the proposed MX-cqca is shown in fig 10 requires four clocking zones and five majority gates for its QCA implementation. MX-cqca has five majority voters. D0, D1, D2 and D3 represent the clocking zones. The truth table represents that

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the MX-cqca is better than the existing Fredkin gate for implementing multiplexer-based designs. It has one less majority gate compared to the Fredkin gate. The QCA layout of the MX-cqca gate is designed using the HDLQ Verilog library for performing the fault testing. QCA layout of the MX-cqca gate has four FOs, one INV, five CWs, eight LSs and five MJs.

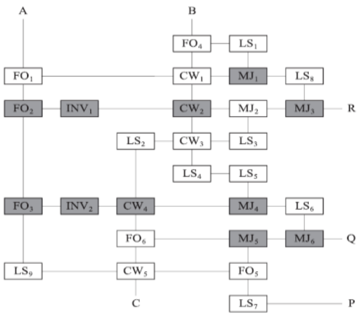

Fig 9. Fredkin gate equivalent circuit

TOFFOLI GATE EQUIVALENT CIRCUIT

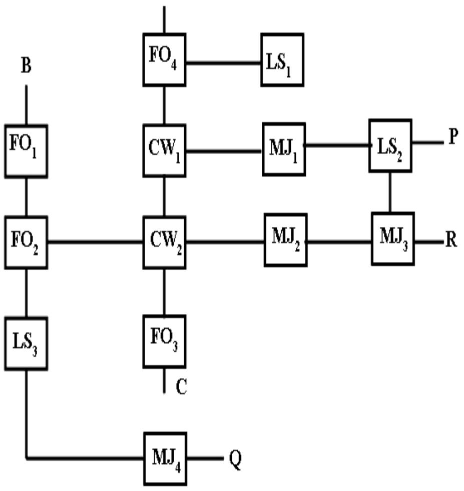

Fig 11.Toffoli gate equivalent circuit

MX-CQCA EQUIVALENT CIRCUIT

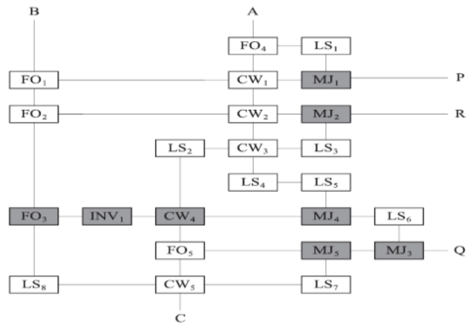

Fig 10.MX-CQCA gate equivalent circuit

In the existing work, equivalent circuit is drawn from QCA layout to obtain the maximum fault coverage. In this paper, the equivalent circuit is obtained from the Boolean expression of Toffoli gate. Fanout (FO) are the components used in equivalent circuit. Cross wire (CW), L-shaped wires (LS), Majority voter (MJ), are the components used in equivalent circuit. Cross wire (CW) is to combine two variables by AND operation. Fanout (FO) is provided in order to drive the output. L-shaped wire (LS) perform the operation in which signal is passed from in and out. Majority voter (MJ) are provided to perform the AND operation. All components combined together in order to perform the maximum fault coverage.

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PERES GATE EQUIVALENT CIRCUIT

In Existing work, MXCQCA and Fredkin gates are drawn in equivalent circuit, from QCA layout. In this paper, the equivalent circuit is drawn from Boolean expression of Peres gate, Fan out (FO), L-shaped wire (LS), Majority voter (MJ), Cross wire (CW) are the components used. Crosswire (CW) is to combine two variable by AND operation. Fanout (FO) is provided to drive the output. Fanout is designed if the fault is 1, the output is inverted. L-shaped wire is to pass the signal from in and out, L-shaped wire is designed in such a way if fault is 1, and output is inverted.

In Majority voter, the output is fault free if the fault is zero, otherwise stuck at fault exists. The output is tested for various combinations of faults in Toffoli gate and Peres gate. Faults are introduced to attain the maximum fault coverage.

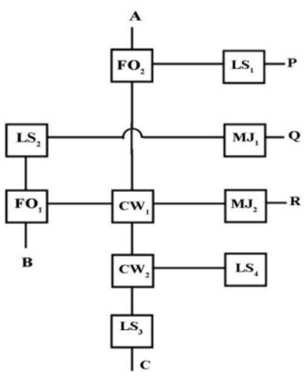

Fig 12. Peres gate equivalent circuit

RESULTS AND DISCUSSION

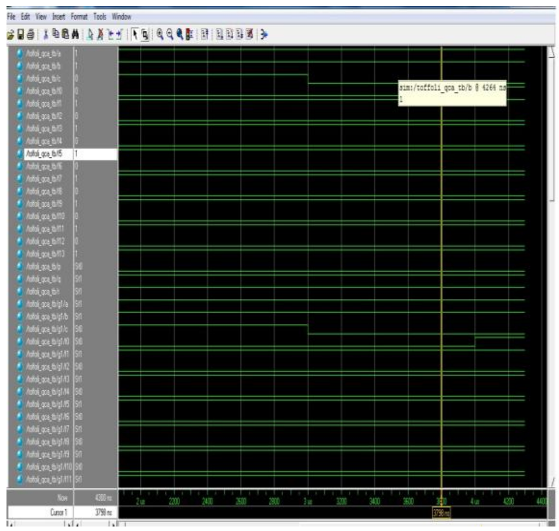

Fig 13.Output waveform of Toffoli gate with fault injection

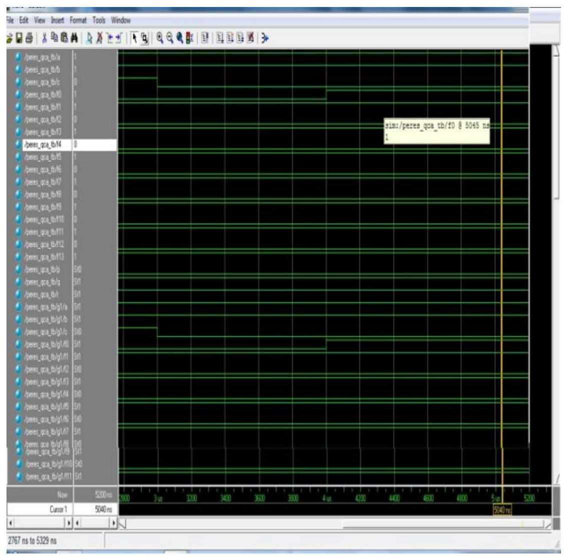

Fig14.Output waveform of Peres gate with fault injection

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Table 5. Comparison table

Reversible gates	Area (No. of slices)	Area (LUT)	Delay (ns)	Power (mw)
Fredkin	16	24	8.560	392.86
MX-CQCA	12	22	8.031	392.86
Toffoli	6	10	6.452	392.86
Peres	6	11	6.452	392.86

CONCLUSION

This paper describes the design of reversible sequential circuits based on two gates, namely Toffoli gate and Peres gate. We have proposed the equivalent Circuit for Toffoli gate and Peres gate in order to less area, computation time and maximum fault coverage. Area, number of gates and timing are analyzed in these gates. Toffoli gate is better in terms of power consumption compared to fredkin gate. In proposed work, Area, number of gates and timing are reduced compared to existing work. In future work, Ultra low power memory circuits and Digital circuits can be designed.

REFERENCES

[1]. Dmitri Maslov, Gerhard W.Dueck, and D.Micheal miller,"Toffoli network synthesis with Templates", 2004

[2]. Vivek V.shende,Aditya K.Prasad,Igor L.Markov and John P.Hayes,"Synthesis of reversible logic circuits",IEEE trans,Vol.22.,No.6.,Jun 2003

[3]. Himanshu Thapiyal and M.B.Srinivas,"A Beginning in the Reversible logic synthesis of sequential circuits", IEEE trans, 2005

[4]. J.E.Rice,"The State of reversible logic synthesis", sep 2005.

[5]. Sivakumar sastry hari,shyam shroff,sk.Noor Mahammad and v.Kamakoti","Efficient building blocks for sequential circuit design",IEEE trans,2006.

[6]. Pallav gupta, Abhinav Agrawal and Niraj k.Jha,"An Algorithm for synthesis of reversible logic circuits", IEEE trans, Vol.25., No.11., Nov 2006.

[7]. Dilip P.Vasudevan, Parag k.lala, Jia Dia, J.Patrick Parkerson,"Reversible logic design with online testability", IEEE trans, Vol.55. No.2, Apr 2006.

[8]. Min-Lun Chuang, Chun-Yao Wang, "Synthesis of reversible sequential elements", IEEE trans, 2007

[9]. Himanshu Thapiyal, Nagarajan Ranganathan,"Reversible logic based concurrently testable latches for molecular QCA", IEEE trans., vol.59, No.1,Jan 2010.

[10]. Sk.Noor Mahammed and Kamakoti veezhinathan,"Constructing online

IJREB

ISSN 2321-743X

International Journal of Research in

Engineering and Bioscience

Volume 2 (Issue 4) Pages (111-121)

Journal home page: www.ijreb.org

testable circuits using reversible logic", IEEE trans., vol.59, No.4. Dec 2010.

[11]. Himanshu Thapiyal and Nagarajan Ranganathan,"Design of reversible sequential circuits optimizing quantum cost, delay and garbage outputs", ACM Journal on emerging tech in computer Systems, vol.6, No.4,Dec 2010.

[12]. Lafifa Jamal,Md.shamsujjoha, and Hafiz Md.Hasan babu," Design of optimal reversible carry look ahead adder with optimal garbage and quantum cost ",International Journal of Engineering and technology, vol.2.,No.1.,Jan 2012

[13]. Bhagya lakshmi HR, Venkatesha MK,"Design of sequential circuit elements using reversible logic gates", International E-conference on Information Technology and Applications, vol.2, May 2012.

[14]. Sheenu Thapar, Parminder kaur, Nidhi syal,"Multiplier circuit based on reversibility principle", An International Journal (ESTIJ), vol.2, No.4, Aug 2012.

[15]. Raghave garipelly, p.Madhu kiran, A.Santhosh kumar,"A Review on reversible logic gates and their implementation", International Journal of emerging Technology & Advanced Engineering, vol.3.,Mar 2013.