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LOW-POWER HIGH SPEED CARRY SKIP ADDER DESIGN USING FEYMAN TOFFOLI GATE

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ABSTRACT

The most timing critical part of logic design usually contains one or more arithmetic operations, in which addition is commonly involved. In VLSI applications, area, delay and power are the important factors which must be taken into account in the design of a fast adder. The carry-skip adder reduces the time needed to propagate the carry by skipping over groups of consecutive adder stages, is known to be comparable in speed to the carry look-ahead technique while it uses less logic area and less power. In this paper, a design of 8-bit Carry Skip Adder by various reversible logic styles is to be compared quantitatively and qualitatively.

KEYWORDS: Low power, High performance, Carry Skip adder, Logic design style, Reversible Logic

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INTRODUCTION

With the increasing level of device integration and the growth in complexity of microelectronic circuits, power dissipation, delay and area has come the primary design goal. The failure mode of high-power circuits relates to the increasing popularity of portable electronic devices. Laptop computers, pagers, portable video players and cellular phones all use batteries as a power source, which by their nature provide a limited time of operation before they require recharging. To extend battery life, low power operation is desirable in integrated circuits. Furthermore, successive generations of applications often require *more* computing power, placing greater demands on energy storage elements within the system. Power dissipation limitations come in two flavors. The first is related to cooling considerations when implementing high performance systems. High speed circuits dissipate large amounts of energy in a short amount of time, generating a great deal of heat as a by-product. This heat needs to be removed by the package on which integrated circuits are mounted. Heat removal may become a limiting factor if the package (PC board, system enclosure, heat sink) cannot adequately dissipate this heat, or if the required thermal components are too expensive for the application [1]. Addition is the most basic arithmetic operation and adder is the most fundamental component of any digital processor.

Depending on the area, delay and power requirements, several adder configurations such as ripple carry look ahead, carry-skip and carry select are available in the literature. The ripple carry adder (RCA) is the simplest adder, but has the longest delay because every sum output needs to wait for the carry-in from the previous adder cell. It uses O(n) area and has a delay of O(n), for an n-bit adder. The carry look-ahead adder has delay $O(\log n)$ and uses $O(n\log n)$ area. On the other hand, the carry skip and carry select adders have $O(\sqrt{n})$ delay and uses $O(n)$ area . Carry skip adders also dissipate less power than other adders due to their low transistor counts and short wire lengths [2].

ARCHITECTURE OF CARRY SKIP ADDER

The carry skip adder provides a compromise between a ripple carry adder and a CLA adder. The carry skip adder divides the words to be added into blocks. Within each block, ripple carry is used to produce the sum bit and the carry. The Carry Skip Adder

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reduces the delay due to the carry computation i.e. by skipping over Groups of consecutive adder stages [6]. If each Ai # Bi in a group, then we do not need to compute the new value of Ci+1 for that block; the carry-in of the block can be propagated directly to the next block. If Ai = Bi = 1 for some i in the group, a carry is generated which may be propagated up to the output of that group. If Ai = Bi = 0, a carry, will not be propagated by that bit location. The basic idea of a carry-skip adder is to detect if in each group all Ai # Bi and enable the block's carry-in to skip the block when this happens as shown in figure1. In general a block-skip delay can be different from the delay due to the propagation of a carry to the next bit position [7][8].

With carry skip adders, the linear growth of carry chain delay with the size of the input operands is improved by allowing carries to skip across blocks of bits, rather than rippling through them.

A. REVERSIBLE LOGIC

Reversible logic has received great attention in the recent years due to its ability to reduce the power dissipation. Quantum arithmetic components need reversible logic circuits for their construction. Reversible logic circuits find wide application in low power digital design, DNA computing, quantum computing and nanotechnology.

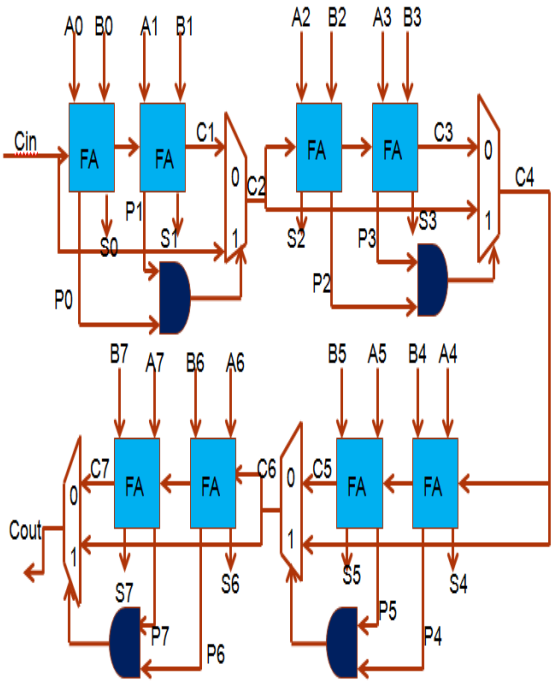

Fig.1 Architectural block of 8-bit Carry Skip Adder (CSKA)

In 1960 R.Landauer demonstrated that high technology circuits and systems constructed using irreversible hardware results in energy dissipation due to information loss. According to Landauer's principle, the loss of one bit of information dissipates kTln2 joules of energy where k is the Boltzmann's constant and T is the absolute temperature at which the operation is performed [4]. Later Bennett, in

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1973, showed that in order to avoid kTln2 joules of energy dissipation in a circuit it must be built from reversible circuits [5] A reversible logic gate is an n- input, n-output logic device with one-to-one mapping. Reversible circuits are constructed using reversible logic gates. These reversible circuits not only produce unique output vector from each input vector but also the input can be reconstructed from the outputs. A reversible circuit should be designed using a minimum number of reversible gates. Fan-out and loops are not allowed in reversible logic circuits [10]. However fan-out and feedback can be achieved by using additional gates. The complexity and performance of the circuit is decided on the following parameter [11][12][13].

(i) Garbage outputs: The number of unused outputs present in the reversible logic circuit. (ii) Number of reversible gates: Total number of reversible gates used in the circuit. (iii) Delay: Maximum number of unit delay gates in the path of propagation of inputs to outputs. It represents the total number of reversible gates used between the primary inputs and the outputs of a reversible logic circuit. (iv) Constant inputs: The number of inputs which are maintained constant at 0 or 1 in order to get the required function. They are necessary to synthesize a reversible function. Fredkin gate: A Fredkin gate [14] in Figure.2 is a conservative-logic gate which maps 3 inputs (X2, X0, and X1) onto 3 outputs (Y2, Y0, Y1). The truth table of a Fredkin gate is given in Tab.1. Roughly speaking, the input *X2* is directly mapped to output*Y2*. When *Y2* =1, inputs *X0* and *X1* are mapped to outputs Y0 andY1, respectively. When X2 =0, on the other hand, the outputs Y0 and Y1 are swapped such that X0 (X1) is mapped to Y1 (resp. Y0). The output is defined by Y2=X2, Y0=X2X0+X2X1 and Y1=X2X1+X2X0. Quantum cost of a Fredkin gate is 5[15].The two input AND gate (AND2) was generated by the FG by grounding one terminal as shown in fig.3.

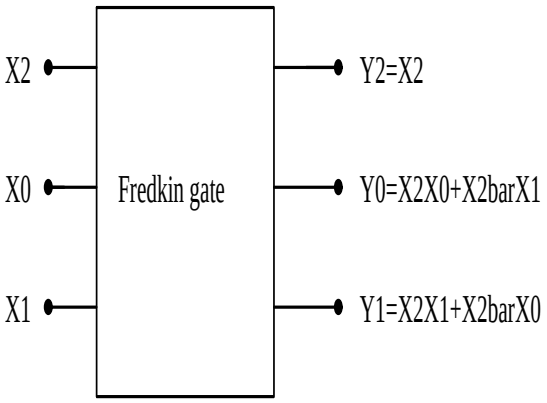

Fig.2 Block diagram of Fredkin Gate

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Table 1: Truth Table of Fredkin gate

Truth Table

X2	X0	X1	Y2	Y0	Y1
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	0	0	1
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	0	1
1	1	0	1	1	0
1	1	1	1	1	1

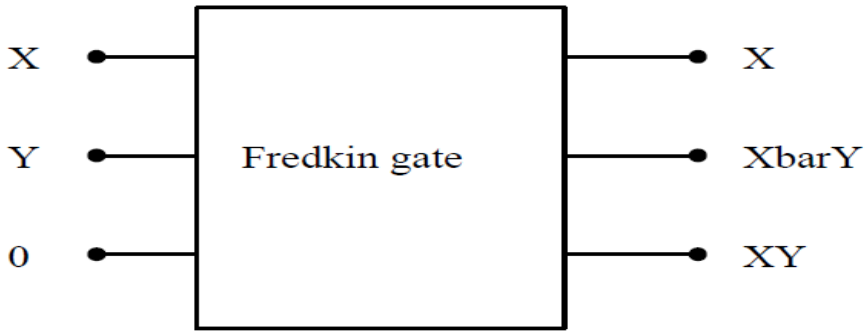

Fig.3 Fredkin gate implementation of AND2 gate

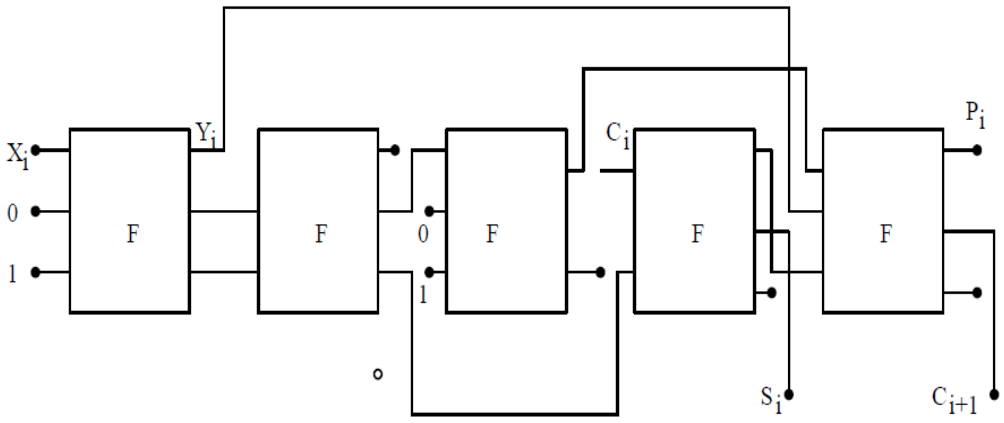

Fig.4 Fredkin Toffoli gate Full Adder

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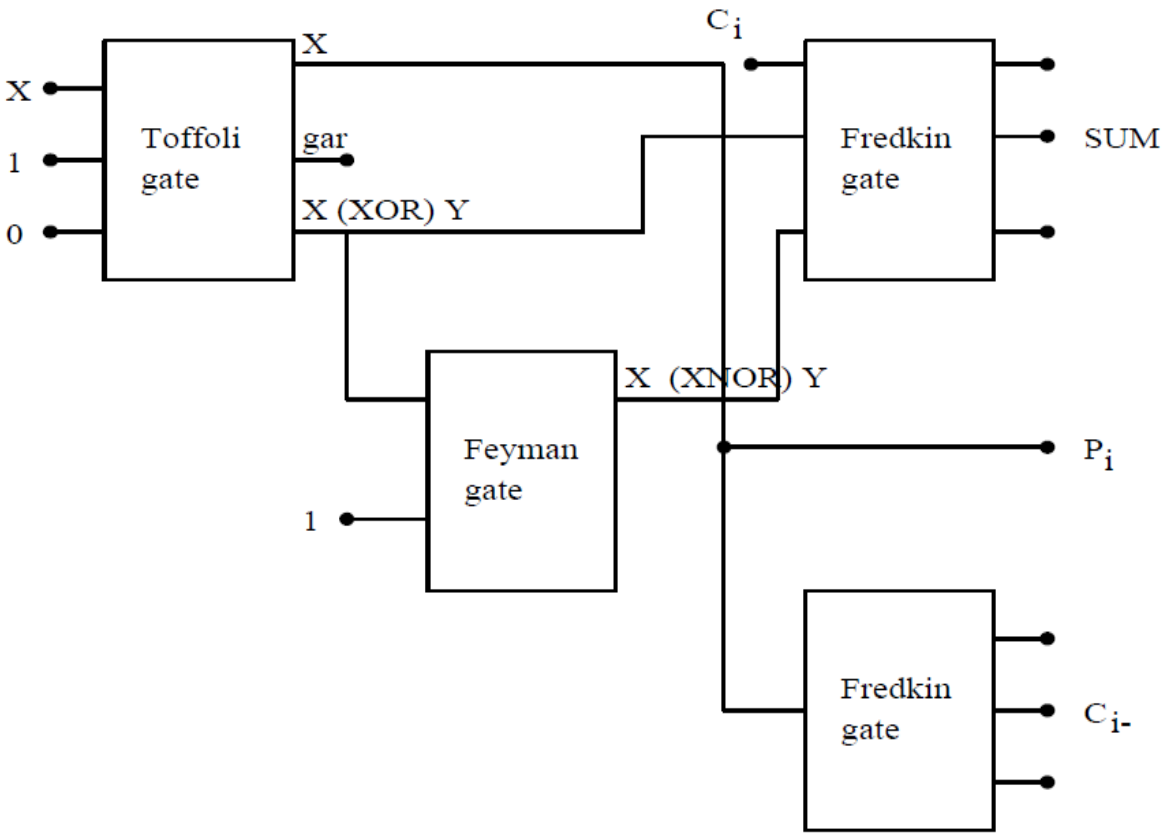

Fig.5 Block diagram of Fredkin gate Full adder avoiding fan-out

The 8- bit Carry Skip Adder is compared based z on the performance parameters like propagation delay, number of transistors and power dissipation. To achieve better performance, the circuits were designed using CMOS process Reversible logic process. The channel width of the transistors is 450nm for the NMOS and 900nm for the PMOS and channel length is 150nm with operating frequency is 10 GHz. All the circuits have been designed using TANNER EDA [16]. With model file as dual.md. The power estimation is a difficult task because of its dependency on various parameters and has received a lot of attention [17].

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Table 2. Comparison of design using reversible logic

Reversible logic style	No. of Transistor	Garbage Output	Power Dissipation (mW)	Propagation Delay (ns)	Power Delay Product (PDP)
Fredkin gate	272	48	0.34mW	16.6ns	5.644pJ
Fredkin toffoli gate feyman gate	260	32	0.18mW	17.2ns	3.096pJ

B. Devices Utilization Summary

Table 3. Summary of Device Utilization

Logic utilization	used	available	utilization
No. of slices	62	768	8%
No. of 4 input LUTs	108	1536	7%
N0. Of bonded IOBs	98	97	100%

Direct Simulation method [18] is used in order to analyze the results. Table 3.Shows Comparative Experimental results of Carry Skip Adder using different Logic Styles in terms of area, power and delay.

RESULT ANALYSIS

It has been observed that Reversible logic using Fredkin Toffoli gate Full Adder (FFA) exhibit better characteristics (speed and Low-Power) as compared to other design styles. So, Reversible logic style can be used where portability and high speed is the prime aim. Where, Reversible logic using Improved Fredkin gate Full Adder (IFFA) consumes the lowest power among the five. With the reduction of Garbage Output, the Improved Fredkin gate Full Adder (IFFA) Reversible logic can be considered best logic design style with respect to all parameters of 8-bit Carry Skip Adder architectures.

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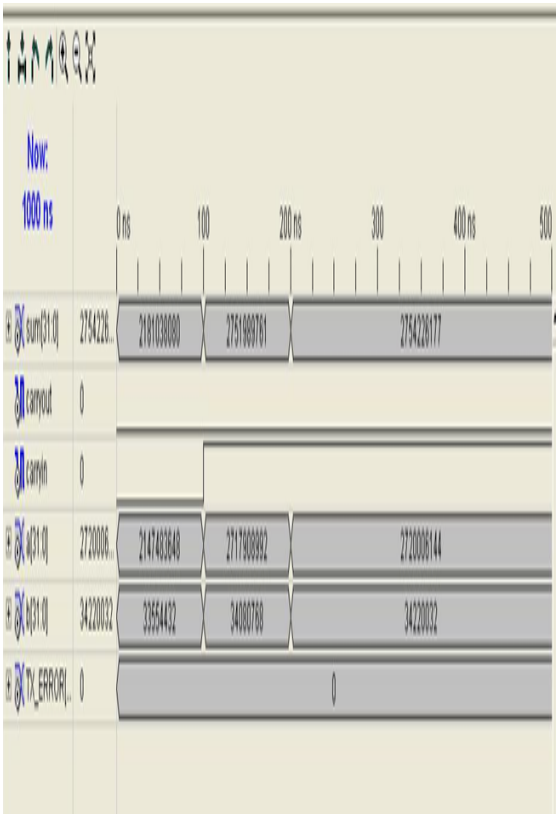

Fig.6 Test bench waveform of 32 bit CSKA

CONCLUSION

In this paper we have designed and simulated 8-bit CSK adder using different reversible logic gates. The novelty of our approach is been justified by the calculated comparison made with that of the results obtained by SPICE simulations.

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